IN THE CLAIMS:

Claim 1. (**Canceled**)

Claim 2. (**Canceled**)

Claim 3. (**Canceled**)

Claim 4. (**Canceled**)

Claim 5. (**Canceled**)

Claim 6. (**Canceled**)

Claim 7. (**Canceled**)

Claim 8. (**Canceled**)

Claim 9. (**Canceled**)

Claim 10. (**Canceled**)

Claim 11. (**Canceled**)

Claim 12. (**Canceled**)

Claim 13. (**Canceled**)

Claim 14. (**Canceled**)

Claim 15. (**Canceled**)

Claim 16. (**Canceled**)

Claim 17. (**Canceled**)

Claim 18. (**Canceled**)

Claim 19. (**Original**) An integrated circuit device, operating in synchronization with a clock signal, comprising:

an internal circuit which, for M external operation cycles ($M \geq 2$), has N internal operation cycles, where N is greater than M ($M < N < 2M$), and wherein

said N internal operation cycles have first internal operation cycles which execute external commands corresponding to said external operation cycles, and second internal operation cycles which execute internal commands.

Claim 20. (**Original**) The integrated circuit device according to claim 19, further comprising:

an internal clock generation circuit which generates an internal clock signal defining said internal operation cycles, according to an external clock signal which defines said external operation cycles; and wherein

said external commands are input in synchronization with said external clock signal, and said internal operation cycles are synchronized with said internal clock signal.

Claim 21. (**Original**) A memory circuit requiring refresh operations, comprising;

a memory core having memory cells;

a memory control circuit which, for M external operation cycles ($M \geq 2$), has N internal operation cycles, where N is greater than M ($M < N < 2M$); and

a refresh command generation circuit which generates refresh commands; and wherein

said N internal operation cycles includes first internal operation cycles which execute external commands corresponding to said external operation cycles, and second internal operation cycles which execute said refresh commands, and

said refresh command generation circuit generates said refresh commands according to a reception of said external command.

Claim 22. **(Original)** The memory circuit according to claim 21, wherein the frequency of said external clock signal is higher than the frequency of said external operation cycles;

further comprising an internal clock generation circuit which generates an internal clock signal defining said internal operation cycles according to the external clock signal; and,

said external commands are supplied according to a cycle which is equal to or greater than said external operation cycle, and are input in synchronization with said external clock signal.

Claim 23. **(Original)** The memory circuit according to claim 22, wherein said refresh command generation circuit permits the generation of said refresh

commands according to the combination of external commands, which are input in synchronization with a prescribed number of said external clock cycles.

Claim 24. (**Original**) The memory circuit according to claim 22, wherein said refresh command generation circuit permits the generation of said refresh commands when said external commands are not input in synchronization with any of the external clock cycles among a prescribed number of said consecutive external clock cycles.

Claim 25. (**Original**) The memory circuit according to claim 22, wherein in cases where the frequency of said external commands is L times the frequency of said external operation cycles, said refresh command generation circuit permits the generation of said refresh commands when said external commands are not input in synchronization with any of (L-1) external clock cycles among said L consecutive external clock cycles, and within said M external operation cycles, combinations of said (L-1) external clock cycles are circulated.

Claim 26. (**Original**) The memory circuit according to claim 22, wherein in cases where the frequency of said external commands is L times the frequency of said external operation cycles,

further comprising:

an internal command register which holds said external commands in the most recent L external clock cycles, and generates corresponding internal commands according to the held external commands; and wherein

in prescribed cycles among said N internal operation cycles, said internal command register ignores the held external commands in some cycles among said L held external commands, and generates said internal commands.

Claim 27. (**Original**) The memory circuit according to claim 26, wherein said refresh command generation circuit permits generation of said refresh commands according to internal commands generated by said internal command register.

Claim 28. (**Original**) The memory circuit according to claim 26, wherein said refresh command generation circuit permits the generation of said refresh commands when there exist no internal commands generated by said internal command register.

Claim 29. (**Original**) The memory circuit according to claims 23 through 28, wherein said refresh command generation circuit generates said refresh commands during a state of permission of said refresh command generation, in response to generation of refresh timer signals generated with prescribed timing.

Claim 30. (**Original**) A memory circuit requiring refresh operations, comprising:

a memory core having memory cells;

a first circuit which receives a command supplied in synchronization with an external clock signal, and which generates a first internal command internally;

a second circuit which generates a refresh command internally in a prescribed refresh cycle which is larger than the cycle of said external clock signal; and

a memory control circuit which includes a first internal operation cycle and a second internal operation cycle shorter than said first internal operation cycle, executes control corresponding to said first internal command according to the first internal operation cycle, and when said refresh command is issued, sequentially executes a control corresponding to the refresh command and a control corresponding to said first internal command according to the second internal operation cycle.

Claim 31. (**Original**) The memory circuit according to the claim 30, wherein the memory control circuit executes the corresponding control according to the first internal operation cycle while a finish timing of the internal operation is faster than a generation timing of the first internal command or the refresh command, whereas, executes the corresponding control according to the second internal operation cycle while 'the generation timing of the first internal command or the refresh command is faster than the finish timing of the internal operation.

Claim 32. (**Original**) An integrated circuit device operating in synchronous with a clock signal, comprising:

a first circuit which generates a first internal command internally according to a command externally received;

a second circuit which generates a second internal command internally, in a prescribed cycle larger than the cycles of an external command cycle; and

an internal circuit which includes a first internal operation cycle according to which an internal operation is executed in synchronous with the external operation cycle, and a second internal operation cycle according to which the internal operation is executed in a shorter cycle than the first internal operation cycle;

wherein the internal circuit executes an operation corresponding to the first internal command according to the first internal operation cycle in a normal state, and executes an operation corresponding to the first and second internal commands according to the second operation cycle during a prescribed period after generation of the second internal command.

Claim 33. (**Original**) A memory circuit requiring refresh operations, comprising:

a memory core having memory cells;

a first circuit which receives external commands supplied with an interval equal to or longer than a minimum external command cycle, and which generates a first internal command internally;

a second circuit control which generates a refresh command internally in a prescribed refresh cycle which is larger than the minimum external command cycle; and

a memory control circuit which executes internal operation corresponding to the first internal command according to an internal operation cycle shorter than the minimum external command cycle;

wherein the memory control circuit executes an internal operation corresponding to said first internal command in response to a timing of the external command while a finish timing of the internal operation cycle is faster than the timing of the external command, and when said refresh command is issued, sequentially executes control corresponding to the refresh command and control corresponding to said first internal command according to the internal operation cycle.

Claim 34. (**Original**) The memory circuit according to claim 33, wherein when the internal operation is finished, the memory control circuit receives the first internal command generated by the first circuit or the refresh command generated by the second circuit, and executes the corresponding internal operation.

Claim 35. (**New**) A memory device receiving external commands supplied with an interval equal to or longer than a minimum external command cycle time, comprising;

a memory core including DRAM cells and having an internal operation cycle time shorter than the minimum external cycle time;

an refresh command generation circuit for internally generating a refresh command for refreshing the DRAM cells; and

a control circuit receiving the external command and the refresh command for controlling the memory core such that

the memory core initiates to execute an internal operation cycle upon a receipt of the external or refresh command in case where the control circuit does not receive the external and refresh commands at the beginning of a command reception period, and

the memory core initiates to execute the internal operation cycle immediately after entering the command reception period in case where the control circuit receives the external or refresh commands at the beginning of the command reception period.

Claim 36. (**New**) The memory device as claimed in claim 35, wherein there is a latent period between a reception timing of the external or refresh command the beginning timing of the command reception period in case where the control circuit does not receive the external and refresh commands at the beginning of the command reception period.

Claim 37. (**New**) The memory device as claimed in claim 35, wherein a plurality of the internal operation cycles are sequentially executed while the control circuit receives the external or refresh commands at the beginning of a command reception period.

Claim 38. (**New**) The memory device as claimed in claim 35, the memory device being an asynchronous type DRAM which is not supplied with an external clock signal.

Claim 39. (**New**) The memory device as claimed in claim 35, wherein the external command is a read command or a write command.

Claim 40. (**New**) The memory device as claimed in claim 35, wherein the refresh command generation circuit generates the refresh command both in a normal operation mode and a power down mode.

Claim 41. (**New**) The memory device as claimed in claim 35, wherein the internal operation cycle includes an activation of a word line, an amplification of bit line voltage, an inactivation of the word line and a precharge of the bit lines.

Claim 42. (**New**) The memory device as claimed in claim 35, wherein the control circuit receives a command reception signal which is generated in response to a precharge signal for precharging bit lines.

Claim 43. (**New**) The memory device as claimed in claim 42, wherein a transition of the command reception signal corresponds to the beginning of the command reception period.

Claim 44. (**New**) The memory device as claimed in claim 35, further comprising;

a command register for storing the external command and supplying the control circuit with the external command.

Claim 45. (**New**) The memory device as claimed in claim 44, wherein the command register is reset upon an initiation of the internal operation cycle.